Verification and Validation of SysML Models

Presenter: Myron Hecht and Jaron Chen

Abstract:

Model Based Systems Engineering depends on correct models. However, thus far, relatively little attention has been paid to ensuring their correctness – particularly for larger system engineering models. This paper describes a methodology for performing verification and validation on models written in SysML. The method relies on a catalog of candidate requirements that can be selected and tailored for a specific project. Many of these requirements can be verified automatically. Examples of diagrams taken from an independently created SysML model of a satellite are presented to show how automated verification can be used to identify non-obvious modeling deficiencies.